CLAIMS

1. A packet switch, comprising:

N input buffer sections, provided for respective N input lines, for storing unicast packets and multicast packets input through corresponding input lines;

a switch section for outputting a unicast packet to any of M output lines to which the unicast packet is transmitted when the unicast packet is input from each of the N input buffer sections, and outputting the multicast packet to a plurality of M output lines to which the multicast packet is to be transmitted when the multicast packet is input; and

a scheduler section for selecting the unicast packet or the multicast packet to be output from each of said N input buffers such that the input lines and the output lines cannot conflict each other for the unicast packet, and such that the input lines cannot conflict each other for the multicast packet.

2. The packet switch according to claim 1,

wherein said switch section comprises:

a first storage section for storing the unicast packet corresponding to each of the M output lines; and

a second storage section for storing the multicast packet corresponding to each of the N input lines.

3. The packet switch according to claim 2,

wherein priority control is performed by dividing for each quality of service said input buffer sections and at least one of the first storage section and the second storage section of said switch section.

4. The packet switch according to claim 2,

wherein said unicast packet or said multicast packet can be stopped to enter said switch section from said input buffer section by issuing a congestion notification from the switch

section to at least one of the input buffer section and the scheduler section when said first storage section or second storage section enters a congestion state.

5. The packet switch according to claim 1,

wherein said scheduler section can reserve a timing at which a packet other than the multicast packet cannot be transmitted through a plurality of destination output lines of the multicast packets, when the multicast packet is inputted from said input buffer section to said switch section.

6. The packet switch according to claim 1,

wherein:

a plurality of switch sections are provided;

one of said switch sections receives a part of a divided unicast packet or multicast packet input through the input line and divided into plural sections; and

said plurality of switch sections concurrently transfer plural pieces of divided data corresponding a packet.

7. The packet switch according to claim 1,

wherein:

a plurality of switch sections are provided,

one of said switch sections receives a unicast packet or a multicast packet input through the input line in plural unit times; and

said plurality of switch sections concurrently transfer different packets.

8. The packet switch according to claim 7,

wherein:

a plural packets forms a frame;

each of the plural packets is assigned a first sequence number for identification of an order of the frame, and a second sequence number for identification of an order of the packet in the frame; and

said packet switch further comprises a frame assembly section for rearranging the packets in the frame based on the second sequence numbers, and rearranging the frames based on the first sequence numbers in the output lines.

9. The packet switch according to claim 7,

wherein:

a plural packets forms a frame;

each of the plural packets is assigned a first sequence number for identification of an order of the frame, and a second sequence number for identification of an order of the packet in the frame; and

a corresponding switch section is instructed to stop transferring operations of packets when a number of frames being rearranged reaches a predetermined value when the packets are rearranged based on the first and second sequence numbers in the output lines.

10. The packet switch according to claim 7,

wherein:

an IP packet having a variable length is formed by said plurality of packets; and

a packet belonging to the same flow is input to the same switch section based on a flow identification of the IP packet in the input lines.